IN THE CLAIMS

Cancel claims 1-24 without prejudice or disclaimer, and add new claims 25-34 as follows:

25. (New) A semiconductor circuit on a semiconductor chip comprising:

a first access port and a second access port; and

a plurality of memory banks which can be accessed through both said first access port and said second access port;

wherein said plurality of memory banks each includes a plurality of word lines, a plurality of bit lines, a plurality of memory DRAM cells, and a sense amplifier circuit, and

wherein one of said first and second access ports has priority over the other of said first and second access ports when said first and second access ports access a same memory bank of said plurality of memory banks.

26. (New) The semiconductor circuit according to claim 25,

wherein said plurality of memory banks each further includes global bit lines coupled to said plurality of bit pairs.

27. (New) The semiconductor circuit according to claim 26, further comprising:

a decision circuit which sets said priority among said access ports.

28. (New) The semiconductor circuit according to claim 27,

wherein said first and second access ports handle different bit widths.

29. (New) The semiconductor circuit according to claim 27, further comprising:

a hit/miss judgment circuit,

wherein said first access port and said second access port handle different bit widths.

30. (New) The semiconductor circuit according to claim 29,

wherein an access to one of said plurality of memory banks through said first access port and an access to another one of said plurality of memory banks through said second access port has an overlapping period.

31. (New) A semiconductor circuit on a semiconductor chip comprising:

a first access port and a second access port;

a plurality of memory banks which can be accessed through said first access port and said second access port;

wherein said plurality of memory banks each includes a plurality of word lines, a plurality of bit lines, a plurality of memory DRAM cells, and a sense amplifier circuit,

wherein one of said first and second access ports has priority over the other of said first and second access ports when there is a conflict between accesses from said first access port and said second access port, and

wherein when an access through said first access port is a miss and an access through said second access port is a hit, data is outputted through said second access port until an output through said first access port is ready.

32. (New) The semiconductor circuit according to claim 31,

wherein said plurality of memory banks each further includes global bit lines coupled to said plurality of bit pairs.

33. (New) The semiconductor circuit according to claim 32, further comprising:

a hit/miss judgment circuit,

wherein said first access port and said second access port handle different bit widths.

34. (New) The semiconductor circuit according to claim 33,

wherein an access to one of said plurality of memory banks through said first access port and an access to another one of said plurality of memory banks through said second access port has an overlapping period.